Development of high-k dielectric for Antimonides and a sub 350ºC III-V pMOSFET outperforming Germanium

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Introduction

$In_xGa_{1-x}Sb$ channel materials have the highest hole and electron mobility among all III-V semiconductors, high conduction and valence band offsets (CBO/VBO) with lattice matched $Al_xIn_{1-x}Sb$ for heterostructure MOSFET design [1] and allow low thermal budget MOSFET fabrication (Figure 1). While buried channel HEMT-like devices with excellent electron and hole transport [3-5] have been demonstrated, realization of an Sb-channel MOSFET has remained elusive due to the highly reactive nature of the Sb-surface (Figure 2). In this paper we overcome these challenges (Figure 1) and fabricate an $In_xGa_{1-x}Sb$ pMOSFET with high hole mobility (μ_h) : a bottleneck for III-V complimentary logic. Synchrotron Radiation Photoemission Spectroscopy (SRPES) is used to aid the development of ALD Al_2O_3 on GaSb with a mid bandgap Dit of $3\times10^{11}/cm^2eV^{-1}$. A p^+/n diode with ideality factor of 1.4 and $I_{ON}/I_{OFF} > 5\times10^4$ is developed. pMOSFETs with various channel configurations to optimize the hole transport are fabricated using a sub 350ºC gate-first process. Surface (buried) channel pMOSFETs with peak μ_h of 620 (910) cm^2/Vs and having more than 50 (100) % higher mobility than Germanium over the entire sheet charge (N_s) range are demonstrated and analyzed.

Process Development

Two key steps in developing a process flow for Sb-MOSFETs are development of a high quality gate-dielectric and diodes for the source and drain.

(a) Dielectric: The effectiveness of different chemical cleans in removing GaO_x and SbO_x on GaSb surface was studied using"nqy "gpgti{"*j Σ? 322gX+"tcf kcvkqp"htqo "vj g"u{pej tqvtqp" which allows observing the top few monolayers of the surface with great accuracy (Figure 3). Only an HCl-based clean is able to effectively reduce both GaO_x and SbO_x, rendering a GaSb surface free of native oxide. RMS roughness just after HCl clean and after 10 cycles of ALD deposition was measured to be 0.66 and 0.73nm respectively (Table 1). Increased photoluminescence (PL) intensity was also observed in a GaSb sample with an HCl-based clean (Figure 4) [6]. The Al_2O_3 bandgap was determined to be 6.3eV from the Al 2p loss spectrum (Figure 5), which agrees well with values reported for ALD Al_2O_3 under similar conditions [7]. As SRPES has a high energy resolution near the valence band spectrum maximum, VBO can be precisely extracted by taking the difference between spectra before/after Al_2O_3 deposition (Figure 6(a,b)). The measured CBO/VBO of 2.48eV/3.1eV for Al_2O_3 on GaSb are sufficient to minimize gate leakage by thermal and tunneling processes, and the insulator is therefore well-suited for a MOSFET design (Figure 6(c)). A 30min/350ºC anneal in forming gas (5/95%:H_2/N_2) greatly improved the dielectric properties (Figure 7). Inversion response at 300K was observed on both n/p-type GaSb (Figure 8). Frequency dispersion in accumulation is less than 1/2.1 %/decade for p/n-type substrate. Dit across the entire bandgap was calculated using the conductance method in the depletion region [8] on n/p-type substrate and varying the temperature from 300-77K (Figure 9). A mid bandgap Dit value of $3\times10^{11}/cm^2eV$ was achieved. The Dit distribution is asymmetric with an order of magnitude higher Dit towards the conduction band, which is in qualitative agreement with the fact that the charge neutrality level of GaSb is located at ~0.1eV from the valence band [9].

(b) Diode: Figure 10 shows the diode characteristics with various Be implant conditions. Sheet resistance decrease with anneal temperature saturates at 340ºC and good diode characteristics with I_{ON}/I_{OFF} of $> 5\times10^4$ and an ideality factor of 1.4 could be obtained with annealing at 350ºC for 30 min (Figure 10). The low temperatures required for S/D activation allows for a self-aligned gate-first process flow while preserving the high quality at the Al_2O_3/GaSb interface. Figure 11 shows the process flow: 100 cycles (~10nm) of ALD Al_2O_3 deposited at 300ºC was used as the gate dielectric followed by Al evaporation and gate patterning. S/D contacts were formed with Ti/Ni liftoff. Fabrication of the transistors was completed with a 350ºC forming gas anneal which also activates the S/D implant. The, temperature during the entire process flow never exceeds 350ºC.

Channel Engineering

Three different structures were explored as shown in Figure 12: a GaSb substrate was first used to optimize the interface with Al_2O_3 and FET characteristics (Figure 12(a)). The top surface is terminated with two monolayers of GaSb in all subsequent structures to maintain the high quality interface with Al_2O_3. A thin (7.5nm) $In_xGa_{1-x}Sb$ channel on a wide bandgap (WB) $Al_{0.80}Ga_{0.20}Sb$ metamorphic buffer grown on GaAs (Figure 12(b)) was used to induce strong confinement that is one contributor to the high mobilities. It also serves to reduce I_{OFF} due to the junction leakage from the large source/drain contacts (Figure 14). A biaxial compressive strain of 0.7% or 1.7% was added to the design by increasing the In fraction in the channel from

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14. ABSTRACT

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$In_{0.20}Ga_{0.80}Sb$ to $In_{0.35}Ga_{0.65}Sb$ to further enhance μ_h and I_{ON} (Figure 14). Buried channel devices with a thin WB $Al_{0.80}In_{0.20}Sb$ cap were also studied in order to isolate the effects of surface roughness and traps in the dielectric on the inversion charge (Figure 12(c), HR-TEM: Figure 13). Figure 15 shows typical output characteristics of an L_G=5μm device: I_{ON}/I_{OFF} is > 10^4, and I_{SUB} and I_G remain orders of magnitude lower throughout the range of operation. Subthreshold Slope (SS) was measured to be 120mV/decade, which is comparable to the theoretical value of 105mV/decade for our gate stack as obtained from a 1D Schrödinger-Poisson simulation with Dit = 0. A 30% increase in I_{ON} is observed in the buried channel device as compared to surface channel (Figure 16). A further 80% increase is obtained with 1% increase in strain in the channel (Figure 17). With 0.7% strain μ_h in the buried (surface) device is higher than Ge (Si) over the entire N_s (Figure 18(a)). Peak μ_h in surface (buried) $In_{0.35}Ga_{0.65}Sb$ channel with 1.7% biaxial compression is > 300 (400)% higher than Ge, and the μ_h gain is maintained over the entire N_s range (Figure 18(b)). The enhancement of μ_h in the buried channel device over the surface channel configuration is maintained at high N_S thanks to the small thickness and high VBO (0.32eV[1]) of the WB cap with the channel which prevents spillover of charge in the cap layer.

Analysis

Pulse-IV measurements which eliminate the influence of traps showed only a 5% increase over DC characteristics for surface $In_{0.35}Ga_{0.65}Sb$ which reduces to 2% for the buried channel device (Figure 19). I_{ON} increases 4X with decrease in temperature from 300 to 80K (due to the μ_h increase) while I_{OFF} decreases by 10^3 (indicating a defect-free diode) (Figure 20). SS scaled linearly with decrease in temperature from 120mV/decade at 300K down to 31mV/decade at 80K, providing another proof that the effect of Dit is minimal in our devices (Figure 20(inset)). The temperature dependence of μ_h was studied for both surface and buried channel device (Figure 21). A T^{-1} dependence at $N_s=5\times10^{12}/cm^2$, characteristic of a mobility limited by interface roughness, is observed in the surface channel device. This changed to a $T^{-1.32}$ dependence for the buried channel which is closer to the $T^{-1.5}$ dependence associated with phonon scattering (Figure 22). This suggests that the μ_h gain in the buried channel device is primarily due to suppression of scattering from the interface roughness which was measured to be higher in our devices as compared to Si/Ge (Table 1). At low temperature when I_{ON}/I_{OFF} becomes $>10^8$, GIDL due to BTBT was observed in the surface channel device (Figure 23). Buried channel device moves the maximum E-field due to V_{GD} in the WB cap (Figure 23(inset)) suppressing BTBT which might be the dominant component of I_{OFF} in scaled devices [10]. Lastly, a 4.3% increase in I_D was observed when 50MPa of uniaxial compression was applied by wafer bending (Figure 24) to an $In_{0.35}Ga_{0.65}Sb$ device with the channel oriented along [110] direction [13]. This gives a r lg| qtguucpeg"eqghhekgpv"*pL) of +0.86/GPa which is higher than the corresponding p_L values of +0.48/0.71/GPa for Ge/Si pMOSFETs, indicating that an even higher enhancement is possible with further addition of uniaxial strain.

Summary

$In_xGa_{1-x}Sb$ pMOSFETs with SS of 120mV/decade, $I_{ON}/I_{OFF}>10^4$ and Gm,max of 140/90 mS/mm (L_G=5μm), fabricated using a self-aligned gate-first process are demonstrated for the first time. Table 2, summarizes the key transistor results. ALD Al_2O_3 with Dit of $3\times10^{11}/cm^2eV$ and strain engineering has enabled a high-mobility $In_xGa_{1-x}Sb$ pMOSFET an important step toward the implementation of III-V CMOS in future technology nodes.

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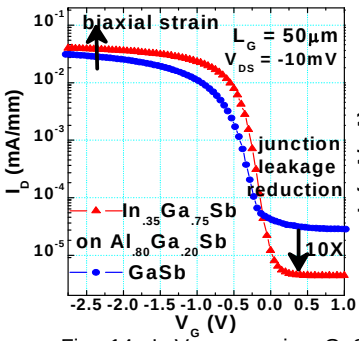


Fig. 14: I_D-V_G comparing GaSb substrate & strained $In_{.35}Ga_{.65}Sb$ on $Al_{.80}Ga_{.20}Sb$.

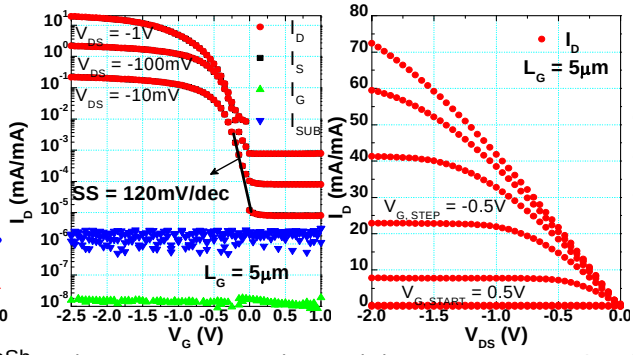


Fig. 15: I_D-V_G & I_D-V_D characteristics on L_G=5um, $In_{.35}Ga_{.65}Sb$ surface channel device.

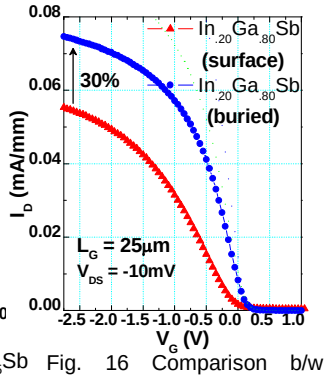


Fig. 16 Comparison b/w buried/ surface channel.

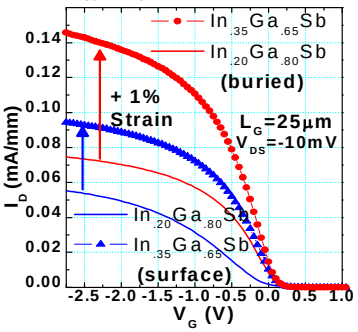


Fig. 17 Comparison b/w 0.7 % strain ($In_{.20}Ga_{.80}Sb$) & 1.7% strain ($In_{.35}Ga_{.65}Sb$) channel.

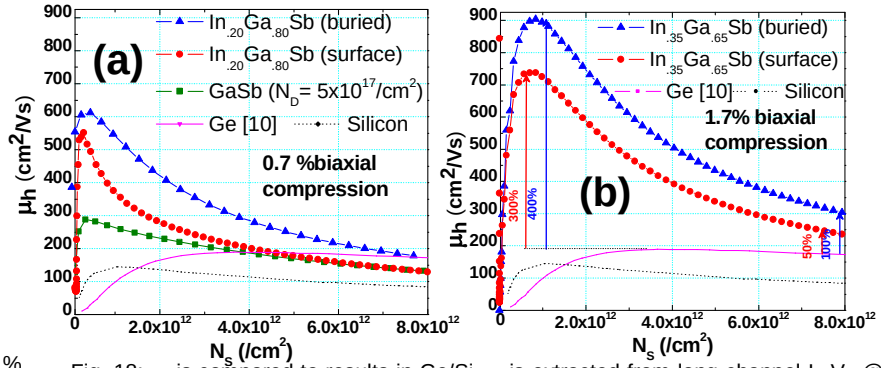


Fig. 18: μ_h is compared to results in Ge/Si. μ_h is extracted from long channel I_D-V_G @ V_{DS}=-10mV & measured Cgc; no corrections for R_{SD}/any other corrections were applied.

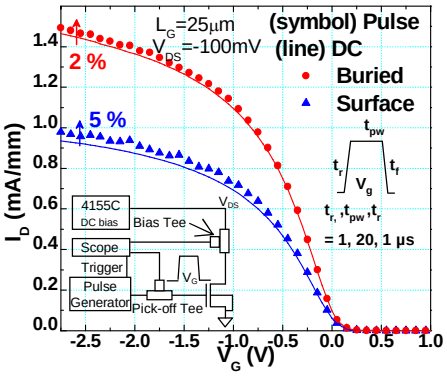


Fig. 19 : Pulse vs. DC IV characteristics.

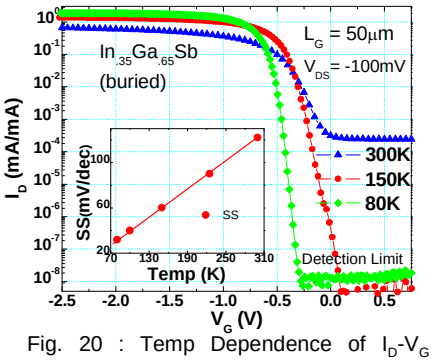


Fig. 20 : Temp Dependence of I_D-V_G (inset : SS with T).

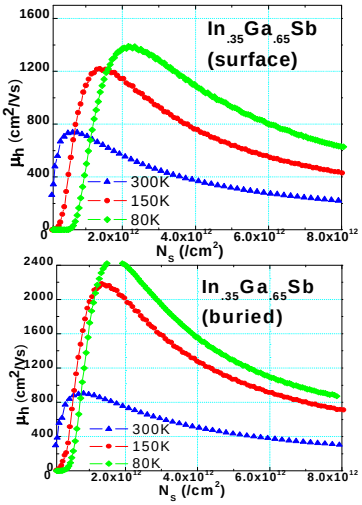


Fig. 21 : Temp Dependence of mobility.

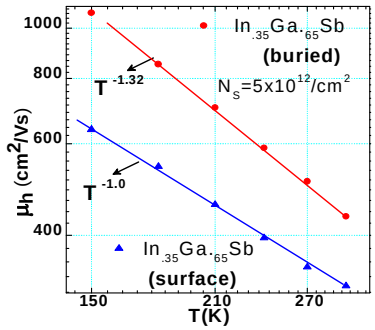


Fig. 22 : Temp dependence of μ_h : buried vs. surface (Interface/phonon limited µ have T^{-1}/$T^{-1.5}$ dependence).

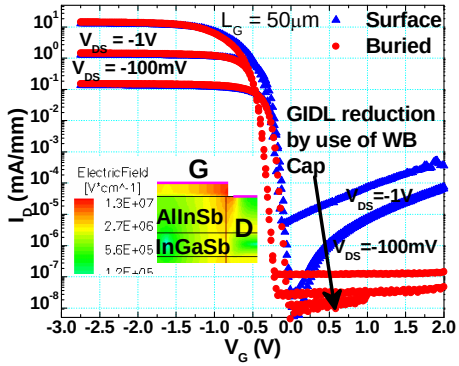


Fig. 23 :GIDL due to BTBT seen in surface channel device at 80K. Use of wide bandgap (WB) cap in buried channel moves the high E-field region in the WB material *note : our junctions were not optimized to cause intentional BTBT.

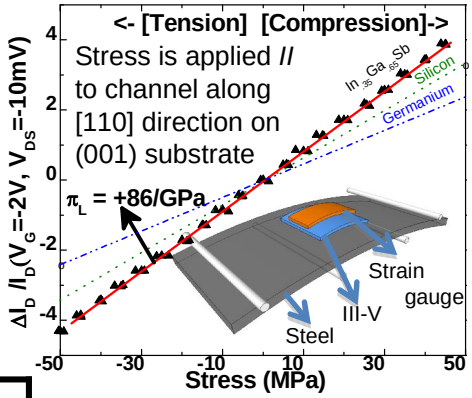


Fig. 24 :High response to uniaxial stress by wafer bending on $In_{.35}Ga_{.65}Sb$ channel suggests an even higher enhancement with uniaxial stress by S/D engineering.

Table 2: Summary of results

	SS mV/dec	$\mu_{h,peak}$ (cm²/Vs)	μ_h N_S=5x10^{12}	$G_{m,max}$ L_G=5µm	I_{ON}/I_{OFF}	Biax. Strain	p_L [110] (001)
Surface ($In_{.35}Ga_{.65}Sb$)	120	620	320	94mS/mm	>10^4	1.7%	+.86/GPa
Buried ($In_{.35}Ga_{.65}Sb$)	125	910	435	140mS/mm	>10^4	1.7%	+.86/GPa

Strengths

- μ_h = 800-950 cm²/Vs (+Strain) [2]
- μ_e = 8-77×10³ cm²/Vs
- High CBO & VBO with lattice matched $Al_xIn_{1-x}Sb$ [1]
- Low temp processing (**Fig. 11**)

Challenges

- Highly reactive surface (**Fig. 2**)
- Need good dielectric on Sb's (**Fig. 8/ Fig. 9**)
- Need diode for S/D (**Fig. 10**)
- No MOSFET processing on Sb (**Fig. 11**)

Fig. 1: Strengths & challenges in development of an $In_xGa_{1-x}Sb$ channel MOSFET.

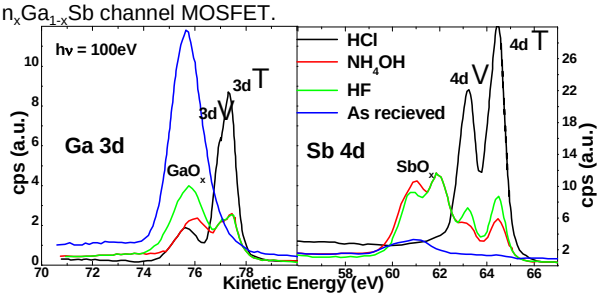


Fig. 3: Effectiveness of (1) HCl (2) HF (3) NH_4OH clean in removing GaO_x/SbO_x is studied using low energy radiation from synchrotron (↑spin up ↓spin down).

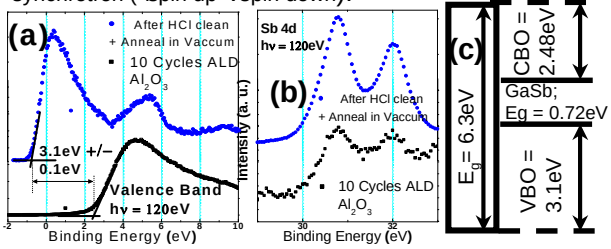


Fig. 6: (a) VBO of Al_2O_3 on GaSb is calculated taking the difference in valence band spectrum [12] (b) Sb 4d peak from the substrate is used for aligning the spectrum (c) Band diagram for Al_2O_3 on GaSb.

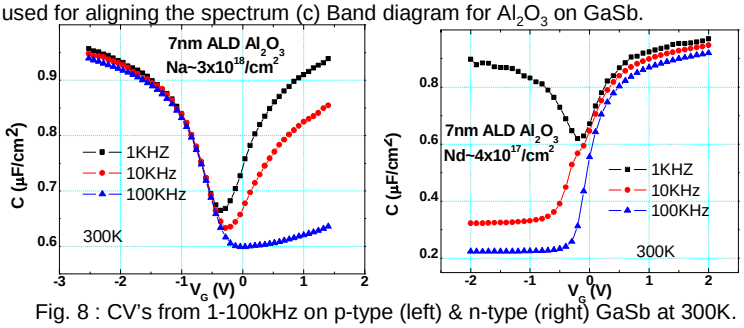


Fig. 8 : CV's from 1-100kHz on p-type (left) & n-type (right) GaSb at 300K.

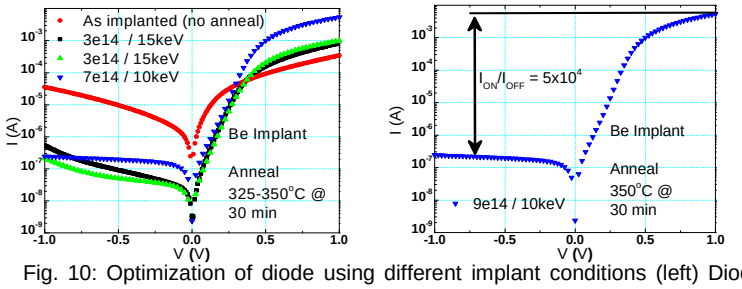
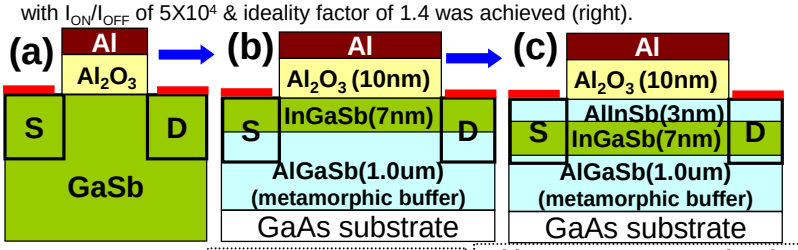


Fig. 10: Optimization of diode using different implant conditions (left) Diode with I_{ON}/I_{OFF} of 5X10⁴ & ideality factor of 1.4 was achieved (right).



- **Optimize diode & dielectric**
- **Introduce Biaxial Strain**
- **Cut Junction Leakage**
- **Thin WB cap to insulate channel from dielectric interface while preventing spillover in WB**

Fig. 12: Different channel designs to separate the impact of different issues & enhance transistor performance. Top surface is terminated with 2 monolayers of GaSb in each case to maintain high quality interface with Al_2O_3.

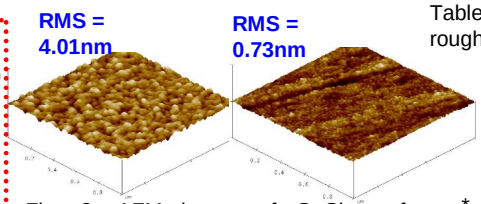


Fig. 2: AFM image of GaSb surface exposed in air for a long time (left); after HCl Clean + 10 cycles ALD (right).

Table. 1 : Surface roughness (nm) comparison.

(100)	GaSb	Si	Ge
Pre Clean	0.36-4.01*	0.28 [9]	0.15 [9]
After oxide	0.73	0.4 [11]	0.1 [11]

* depending on time exposed to air

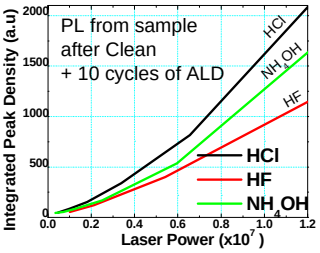


Fig. 4 : Higher PL response with HCl clean indicates a better interface [6].

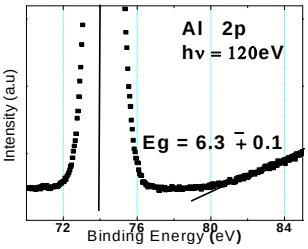


Fig.5 : Bandgap is calculated from the Al 2p loss spectrum [12].

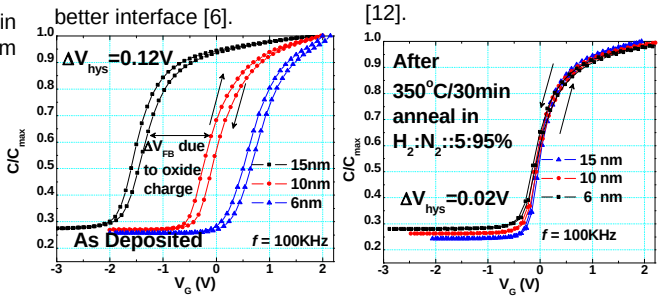


Fig. 7 :Bidirectional CV characteristics after anneal in forming gas show reduced hysteresis/stretch-out and confirm removal of oxide charge.

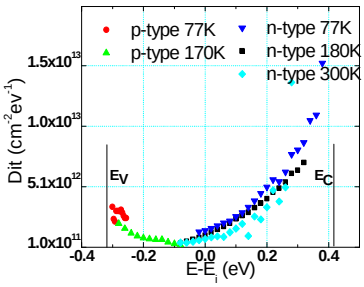


Fig. 9 : Dit distribution is calculated across the bandgap using conductance method [6] on p/n-type substrate over T=300-80K. Mid bandgap Dit of 3×10¹¹/cm²eV is achieved.

- Field oxide deposition + Active area etch
- HCl based clean + 100 cyl. ALD Al_2O_3 @ 300ºC (~10nm) as gate dielectric
- Aluminum evaporation + Gate patterning
- Be implant(9e14dose/10keV)+S/D liftoff (Ti/Ni)
- 350ºC/30min forming gas anneal

Fig. 11: Self-aligned gate-first process flow.

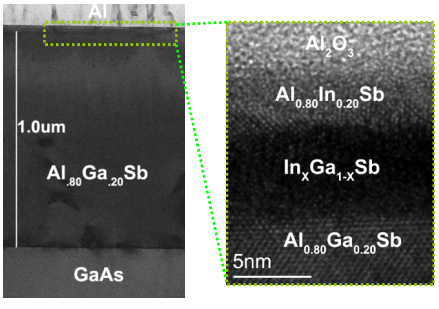


Fig. 13 HR-XTEM of buried channel device (left) Zoomed picture of gate stack (right). Sharp interfaces are observed between all layers.